

STRUCTURE OF A CMOS IMAGE SENSOR

BACKGROUND OF THE INVENTION

5 Field of Invention

[0001] This invention relates to a structure of a photodiode image sensor device.

More particularly, the present invention relates to a structure of a CMOS image sensor (CIS).

10 Description of Related Art

[0002] A photodiode image sensor device is the most commonly used device for detecting images. A typical photodiode image sensor device comprises a reset transistor and a light sensor region formed by a photodiode. For example, a photodiode is formed with an N type doped region and a P type substrate. When the photodiode image sensor is in operation, a voltage is applied to the reset transistor gate to turn on the reset transistor and to charge the N/P diode junction capacitor. The reset transistor is turned off when the charging of the N/P diode junction capacitor has reached a certain high voltage. The N/P diode generates a reverse bias to form a depletion region. When a light is shinned on the N/P diode light sensor, electrons and holes are generated. These holes and electrons are separated by the electrical field of the depletion region, causing the electrons to travel in the direction of the N-type doped region to lower the voltage of the N-type doped region, whereas the holes travel in the direction of the P-type substrate.

[0003] A charge coupled device (CCD) has a high dynamic range and a low dark current. The sophistication of the current technology of a charge coupled device allows

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the charged couple device to become the most popular image sensing device. The manufacturing for a charge coupled device is, however, rather special. The price for a CCD is therefore very high. Moreover, the driver requires a high voltage operation, leading to the problems of high power dissipation and inability of random access of
5 memory.

[0004] A CMOS image sensor has the characteristics of high quantum efficiency, low read noise, high dynamic range and random access, and it is one hundred percent compatible with the manufacturing for a CMOS device. A CMOS image sensor can combine with other control circuit, A/D converter and several signal processing circuits
10 on a single wafer to achieve the so-called system on a chip (SOC). The progress of the technology of a CMOS image sensor, therefore, greatly reduces the cost of an image sensor device, the picture size and the power of dissipation. The CMOS image sensor is therefore slowly replacing the charge coupled device.

[0005] The structure of a conventional CMOS image sensor is summarized in the
15 following.

[0006] Referring to Figure 1A, a field oxide layer 102 is formed on a substrate 100. A reset transistor 120 that comprises a gate oxide layer 104 and a polysilicon gate 106 is formed on the substrate 100. The source/drain region 108 and the doped region 112 of the photodiode sensor region 110 are formed by implanting and thermal driving-in ions using
20 the field oxide layer 102 and the polysilicon gate 106 as masks. A spacer 114 is formed on the sidewalls of the polysilicon gate 106 and the gate oxide layer 104. A self-aligned block (SAB) 116 is further formed on the photodiode sensor region 110 to complete the formation for a CMOS image sensor device.

[0007] The conventional CMOS image sensor, however, has the following problems.

[0008] After the above CMOS image sensor is formed, the backend process is conducted, such as the formation of the inter-layer dielectrics and metal conductive line, 5 which are used for the controlling of the device. The application of plasma etching is inevitable in the backend process for, for example, the defining of the contact/via opening or the metal conductive line. The high power plasma, however, can penetrate the inter-layer dielectrics to induce damages on the surface of the photodiode. The damages inflicted upon the surface of the photodiode due to plasma etching are especially 10 prominent in the vicinity of the bird's peak region. As a consequence, current leakage occurs more easily in the photodiode sensor region. The aforementioned current leakage problem would cause the CMOS image sensor to generate a significant dark current, leading to an increase of read noise.

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SUMMARY OF THE INVENTION

[0009] The present invention provides a structure of a CMOS image sensor, wherein there is a protective layer formed on the CMOS image sensor before the backend process to prevent the CMOS image sensor from being damaged by plasma.

[0010] The present invention provides a structure of a CMOS image sensor, 20 wherein the dark current problem of the CMOS image sensor is greatly mitigated.

[0011] The present invention provides a structure of a CMOS image sensor, which includes a photodiode sensor region, a transistor device region, a transistor, a self-aligned block and a protective layer. The photodiode sensor region and the transistor device region are formed in a substrate, and a self-aligned block is formed on the photodiode

sensor region. A protective layer is formed on the entire substrate, covering the self-aligned block.

[0012] Accordingly, one aspect of the present invention is to provide a protective layer to cover the entire substrate after the manufacturing of the CMOS sensory device.

5 The photodiode sensor region is thus protected from being damaged during the subsequent backend process to minimize the generation of dark current.

[0013] Moreover, besides protecting the photodiode sensory region, the protective layer formed on the entire substrate also protects other regions from being damaged by plasma etching.

10 [0014] Additionally, the protective layer and the self-aligned block comprise different refraction indices. As the incident light penetrates the surface of the photodiode sensor region, the incident light is refracted by the protective layer and the self-aligned block, which are of different refraction indices. The convertibility into photoelectrons of the light absorbed by the photodiode, after being refracted by the two layers of different refraction indices, is better. In other words, quantum efficiency is higher.

15 [0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

20 BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0017] Fig. 1 is a schematic, cross-sectional view of the structure of a conventional CMOS image sensor.

[0018] Figs. 2A through 2E are schematic, cross-sectional views, illustrating the structure and the successive steps of fabricating a CMOS image sensor according to a 5 preferred embodiment of the present invention.

[0019] Fig. 3 is a schematic diagrams illustrating incident lights entering a CMOS image sensor according to a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

10 [0020] Referring to Figure 2E, the CMOS image sensor of the present invention comprises a photodiode sensory region 240, a transistor device region 250, a transistor 230, a self-aligned block 224 and a protective layer 228.

15 [0021] The above photodiode sensory region 240 and the transistor device region 250 are formed on a substrate 200 and are isolated by an isolation layer 202. A channel isolation region 204 is further formed under the isolation layer 202.

20 [0022] The transistor 230 is, for example, a reset transistor or a transmission transistor, which includes a gate oxide layer 206a, a gate conductive layer 208a, a spacer 216 and a source/drain region 220. The gate oxide layer 206a and the gate conductive layer 208a are formed on the transistor device region 260. The spacer 216 is formed on the sidewalls of the gate oxide layer 206a and the gate conductive layer 208a, wherein the source/drain region 220 is formed in the transistor device region beside both sides of the spacer 216.

[0023] The gate oxide layer 204a is formed with, for example, silicon oxide by thermal oxidation. The gate conductive layer 206a is formed with, for example,

polysilicon, polycide formed with polysilicon and metal or metal. The gate conductive layer 206a is formed by, for example, chemical vapor deposition or sputtering. When the gate conductive layer 208 is polysilicon, it is preferably to form a silicide layer 226 on the gate conductive layer 208a and the source/drain region 220 to lower the sheet resistance.

5 The silicide layer 226 includes those formed with a refractory metal, such as titanium silicide or cobalt silicide, and is formed by a salicide process.

[0024] The photodiode sensory region 240 is formed with a heavily doped region 222 and the substrate 200. The dopant type for the heavily doped region 222 is same as that for the source/drain region 220. When the dopant for the substrate 200 is a p-type dopant, the dopant for the heavily doped region 222 is an n-type dopant. If the dopant for the substrate 200 is an n-type dopant, the dopant for the heavily doped region 222 is thereby a p-type dopant. According to the manufacturing process for a CMOS device, the photodiode sensory region 240 is also formed with a heavily doped region 222 and a doped well (not shown in Figure) formed between the heavily doped region 222 and the substrate 200. Therefore, the dopant type for the heavily doped region 222 includes the same type for the substrate 200.

[0025] The self-aligned block 224 is formed on the photodiode sensory region 240. The self-aligned block 224 includes silicon oxide formed by plasma enhanced chemical vapor deposition.

20 [0026] The protective layer 228 is formed on the entire substrate 200, covering the self-aligned block 224 and the transistor 230. The protective layer 228 includes silicon nitride, formed by, for example, plasma enhanced chemical vapor deposition.

[0027] Figures 2A to 2E illustrates the manufacturing of the above CMOS image sensor.

[0028] Referring to Figure 2A, an isolation layer 202 is formed on the substrate 200 to define the photodiode sensory region 240 and the transistor device region 250, wherein a channel stop region 204 is formed under the isolation layer 202. The isolation layer 202, such as, a silicon oxide type of field oxide layer, is formed by, for example, local oxidation. An insulation layer 206 and a conductive layer 208 are sequentially formed on the substrate 200, wherein the insulation layer 206 is, for example, silicon oxide, formed by methods such as thermal oxidation. The conductive layer 208 is, for example, polysilicon, polycide formed with polysilicon and metal or metal, and is formed by methods such as chemical vapor deposition or magnetron DC sputtering.

[0029] Continuing to Figure 2B, photolithography and etching are performed to define a conductive layer 208 and an insulation layer 206 to form a gate conductive layer 208a and gate oxide layer 206a of a transistor in the transistor device region 250. Thereafter, a light ion implantation 210 is conducted on the substrate 200 using the isolation layer 202 and the gate conductive layer 208a as masks. A lightly doped drain region 212 is formed in the substrate 200 on both side of the gate conductive layer 208a and the gate oxide layer 206a. A lightly doped region 214 is also formed in the photodiode sensory region 240. Depending on the dopant type of the substrate 200 is a p-type or an n-type, the dopant for the light ion implantation process 210 is an n-type phosphorus or arsenic, or a p-type boron.

[0030] Referring to Figure 2C, a spacer 216 is formed on the sidewalls of the gate conductive layer 208a and the gate oxide layer 206a. The spacer 216, such as a silicon oxide layer, is formed by, for example, chemical vapor depositing a silicon oxide layer on the substrate 200, followed by anisotropic etching the silicon oxide layer to form a spacer 216. A heavy ion implantation 218 is further conducted to form a source/drain region 220

in the substrate beside the side of the spacer 214 and to form the heavily doped region 222 in the photodiode sensory region 240. The fabrication for a transistor 230 in the transistor device region 250 is thus completed. Depending on the dopant type of the substrate 200 is a p-type or an n-type, the dopant for the high ion implantation process 5 218 is an n-type phosphorus or arsenic, or a p-type boron.

[0031] Referring to Figure 2D, a self-aligned block 224 is formed on the photodiode sensory region 240, wherein the self-aligned block 224 includes a silicon oxide layer and is formed by, for example, chemical vapor deposition. A silicon oxide layer (not shown in Figure) is formed on the substrate, followed by removing the silicon 10 oxide layer in the salicide region, for example, in the transistor device region 250. The silicide layer 226 is formed on the gate conductive layer 208a and the source/drain region 220 in the transistor device region 250.

[0032] As shown in Figure 2E, a protective layer 228 is formed on the substrate, wherein the protective layer 228 covers the regions include the photodiode sensory region 240, the transistor device region 250 and peripheral circuit region (not shown in Figure). 15 The protective layer 228, such as silicon nitride, is formed by, for example, plasma enhanced chemical vapor deposition using silane and ammonium as processing gas.

[0033] After the formation of the CMOS image sensor, a protective layer 228 is formed to cover the entire substrate 200 to prevent damages being induced upon the 20 photodiode by plasma etching in the subsequent backend processing.

[0034] Moreover, this protective layer 228 is formed on the entire substrate 200. In addition to provide a protection for the photodiode sensory region 240, other regions are also protected from being damaged by plasma etching.

[0035] Referring to Figure 3, Figure 3 is a schematic diagram illustrating a part of the photodiode shown in Figure 2E. The protective layer 228 is silicon nitride and the self-aligned block 224 is silicon oxide and the two layers comprise different refraction indices. As the incident light penetrates the surface of the photodiode sensory region, the 5 incident light is refracted by the protective layer and the self-aligned block, which are of two different refraction indices. The convertibility into photoelectrons of the light absorbed by the photodiode, after being refracted by the two layers of different refraction indices, is better. In another words, quantum efficiency is higher.

[0036] Based on the foregoing, the present invention provides a formation of a 10 protective layer to cover the CMOS photodiode image sensor. The photodiode sensory region is thus protected by the protective layer and is prevented from being damaged by plasma etching in the backend process. The generation of dark current is thus reduced to the minimum.

[0037] Moreover, the protective layer is formed on the entire substrate. Therefore, 15 other regions are also protected from being damaged by plasma etching in addition to the photodiode sensory region.

[0038] The protective layer and the self-aligned block comprise different refraction indices. As the incident light penetrates the surface of the photodiode sensory region, the incident light is refracted by the protective layer and the self-aligned block, 20 which are of different refraction indices. The convertibility into photoelectrons of the light absorbed by the photodiode, after being refracted by the two layers of different refraction indices, is better. In another words, quantum efficiency is higher.

[0039] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from

the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.